Microwave Wide-Band Model of GaAs Dual Gate MESFET's

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Abstract—**A multioctave model of GaAs dual gate MESFET's is presented. It consists of 28 frequency independent elements and is valid between 2 and 11 GHz. Dual gate FET's with and without intergate ohmic contact have been considered. The modeling method utilized consists in separate dc and HF characterization and equivalent circuit determination of the active device parts in their actual bias conditions. Thereby, two goals are obtained : a) The topology of the overall model can be derived from well-known simpler, partial ones; and b) the starting values of optimization are precise enough to allow reliable physical solutions.**

I. Introduction

THE DIFFICULTY OF an efficient optimization in determining wide-band equivalent circuits of multiport devices is due to the large number of elements and to an uncertainty that the overall concept of an appropriate equivalent circuit cannot always be supposed to be well known. If the number of elements is of the order of 25 or more, as is the case for dual gate FET's, or FET's with more than two gates, a direct optimization by means of a computer makes no sense, because the error function can have several local minima with physically nonacceptable values of the elements. Precise starting values for the optimization must be found, and this is possible using a method of separate dc and HF characterization of each active device part. In the case of GaAs dual gate FET's, design of the corresponding gain, mixing [1], [2], phase controlling [3], or oscillating [4] circuits will be possible to optimize and the understanding of the functions will be deepened. In any case, the method remains valid for multigate FET's as well as for further multifunctional active microwave devices.

For dual gate FET's, an equivalent circuit has in principle been proposed previously [5], [6], being composed of two single gate FET equivalent circuits but without specific element values and validity frequency range. Recently [7], a dual gate FET equivalent circuit was determined from measured two-port S-parameters assuming the two single gate FET parts to be equal, but that is not necessarily correct in normal use. If typical element values of two single gate FET's inserted into a dual gate FET equivalent circuit are used, an unacceptable deviation from measured S-parameters is obtained.

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The proposed method consists in characterizing each FET part separately in its actual bias conditions, and this is possible using the multidimensional transfer-characteristic (in the case of dual gate FET's, bidimensional) of the device.

In Section II, the detailed dc analysis and characterization will be described and the dual gate FET equivalent circuit will be presented generally in Section III. Section IV is dedicated to the important procedure of the determination of starting values while the optimization results and discussion will be presented in Section V. Section VI is the summary.

II. Transfer DC Characteristics of the Dual Gate MESFET

The dc behavior of the dual gate FET can be described as that of a cascode of two single gate FET's [5], [6]. Fig. 1 shows the symbolic splitting of a dual gate FET into two single gate devices. Normally used dc output characteristics as well as corresponding calculations are unwieldy and need many technological details [5], [6]. A true transfer characteristic $I_D(V_{G1S}, V_{G2S})|V_{DS}=\text{const}$ has recently been reported by the authors [8]. The problem is due to the unknown potential of floating point D_1. From Fig. 1, we deduce

$$I_D = I_{D1} \tag{1}$$

$$V_{DS} = V_{D1S} + V_{DD1} \tag{2}$$

$$V_{G2D1} = V_{G2S} - V_{D1S}. \tag{3}$$

The dual gate FET transfer characteristic can now be constructed using these relations and the dc output characteristics of the two single gate FET parts of the dual gate FET drawn inversely because of (1) and (2) as shown in Fig. 2. The vertical traces $V_{G2S}=\text{const}$ can be constructed using (3) and the fact that the voltage on the horizontal axis is equal to V_{D1S}. Fig. 2 gives such a transfer characteristic of a dual gate FET for $V_{DS}=5$ V.

Taking as an example external bias of $V_{DS}=5$ V, $V_{G1S}=-1$ V, $V_{G2S}=+2$ V corresponding to point P_1 in Fig. 2, we deduce $I_D=34$ mA, $V_{G2D1}=-0.16$ V, $V_{D1S}=2.1$ V, and $V_{DD1}=2.9$ V, and we conclude that both FET parts are saturated. The use of points P_2 and P_3 in Fig. 2 indicate the method used to measure the S-parameters of each FET part and will be discussed in Section IV-C.

Measuring of the output characteristics of each partial

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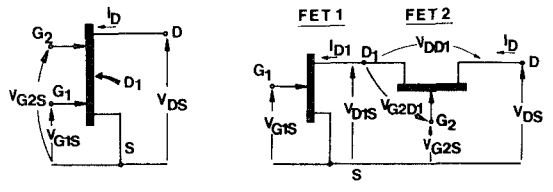

Fig. 1. Treatment of dual gate FET's as a cascode of two single gate FET's for dc analysis reasons.

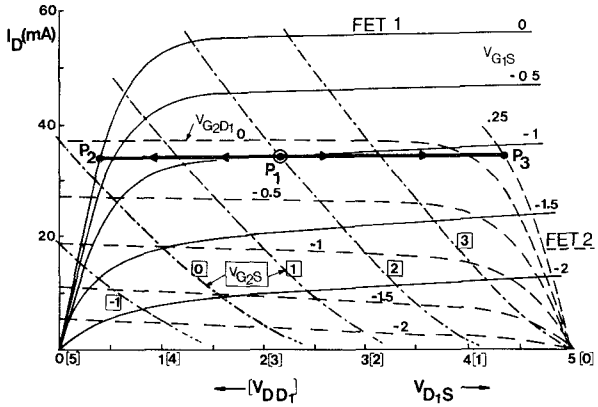

Fig. 2. DC bidimensional transfer characteristic of GaAs dual gate MESFET. Gate 1 : 0.8 μm, gate 2 : 2 μm, gate width: 200 μm.

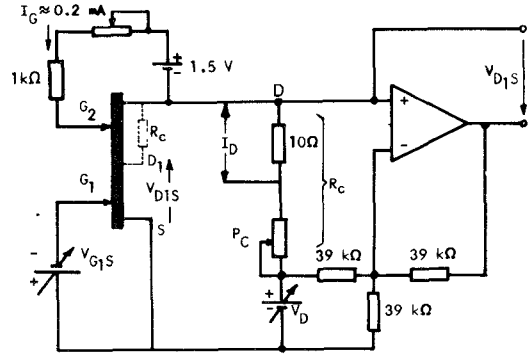

Fig. 3. Measuring setup for dc output characteristics of intrinsic single gate FET parts of dual gate FET. The potentiometer P_c is adjusted to make $R_c' = R_c$, where R_c is the channel resistance of the nonsaturated dual gate FET part. The internal voltage V_{D1S} appears at the output of the operational amplifier and the FET current I_D can be measured across a fixed resistance of 10 Ω.

single gate FET can be done if the gate diode of the other FET is positively polarized. Corrections of the voltage drop across the open channel resistance R_C of this last FET can be made electronically using a measuring setup as illustrated in Fig. 3. R_C can be estimated from

$$R_C \approx \frac{l_2}{l_1 + l_2} \cdot \frac{\Delta V_{DS}}{\Delta I_D}\bigg|_{\substack{V_{G1S} = V_{G2S} \approx 0.8\text{V} \\ V_{DS} \to 0}} \tag{4}$$

with l_1, l_2 being the channel lengths of the corresponding FET's including feed paths.

The characteristics of FET 2 can be measured by exchanging D, S, G_1, and G_2 because of the noncorrectable influence of R_C on the saturation current if it represents a source resistance.

III. Principal Equivalent Circuit

Two types of dual gate MESFET's have been analyzed with different cross sections, as given in Fig. 4(a) and (b). The first one (Fig. 4(a)) has been designed and realized at the Institute of Semiconductor Electronics of the Technical University of Aachen for mixer applications. The second one (Fig. 4(b)), designed and fabricated at the Laboratoires d'Electronique et de Physique Appliquée has an intergate ohmic contact due to the used self-alignment fabrication technique. This 10-μm long ohmic contact forms a dc and HF short-circuit for the active layer beneath and compensates the disadvantage of the long distance between the two gates ($l_{G1G2} \sim 12$ μm) as will be shown in Section V.

The principal small signal equivalent circuit of the dual gate FET has been composed as a cascode of two single gate FET's and can be used for both types of device. This is allowed if the two FET's can be regarded as being decoupled. For FET (b) (Fig. 4(b)), this is evident, while for FET (a) (Fig. 4(a)) this will also be the case even if the space charge layer of the first gate extends 1 μm over the end of gate 1 towards gate 2. Though, for dual gate structures with gate 1 to gate 2 spacing less than 1 μm, such an interaction of the two space charge layers might become important.

The equivalent circuit can be deduced on the basis of a schematical cross section of the dual gate FET, as shown in Fig. 5. It contains 28 frequency independent elements. The dual gate FET is regarded as a three-port device, where gate 2 is not always HF short-circuited [5]. On the contrary, this port can be terminated in order to realize particular circuits [9], [10], or it can serve even as the input HF port [11].

Consequently, we used measured 3-port S-parameters for our optimization. The elements of the equivalent circuit in Fig. 5 partly include parasitic components due to device imperfection or mounting. A separation in element blocks according to their origin is given in Fig. 6: block A includes the intrinsic FET parts; block B includes the parasitic elements of each FET; and block C includes the parasitic elements imposed by the mounting (bonding) of the device and the test circuit interelectrode capacitances.

The origin and principal values of the elements of groups A, B, C is known from the literature [12], [13]. It won't therefore be necessary to repeat this here in detail.

The intrinsic FET's are described by the classic method [14], but the existence of the channel to drain capacitance [15] C_{DC} has also been considered. We found that there is only a small difference in terms of calculated S-parameters between the two device descriptions, especially since in our case the capacitances C_{D1} and C_{D2} have almost the same meaning as C_{DC}, physically as well as electrically, for frequencies up to 12 GHz. Coupling between the two gates has been simulated by the resistance of the active layer R_{12}

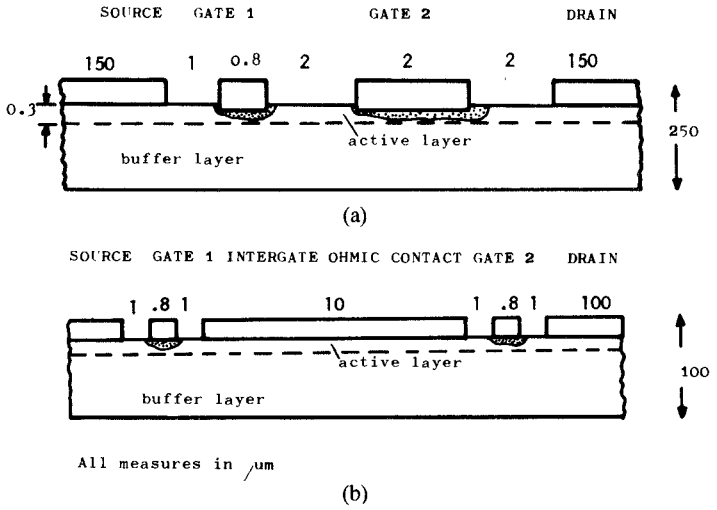

Fig. 4. Principal cross sections of investigated GaAs dual gate MESFET's. Gate width: Type (a): 200 μm, type (b): 150 μm.

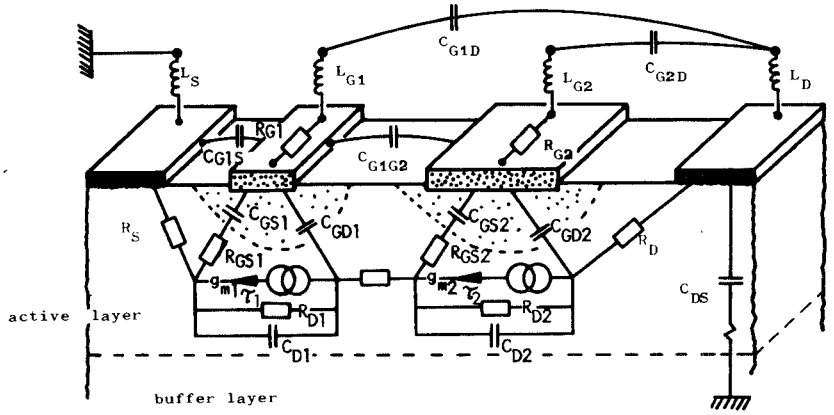

Fig. 5. Schematic cross section of dual gate MESFET of type (a) with implemented equivalent circuit elements.

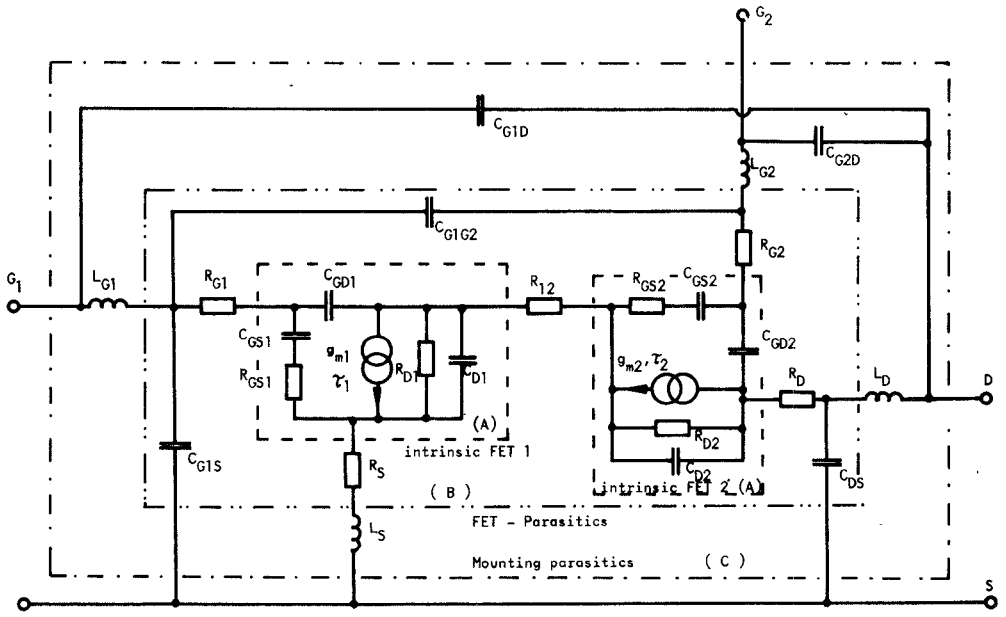

Fig. 6. Equivalent circuit of GaAs dual gate MESFET with elements separated in groups according to their origin.

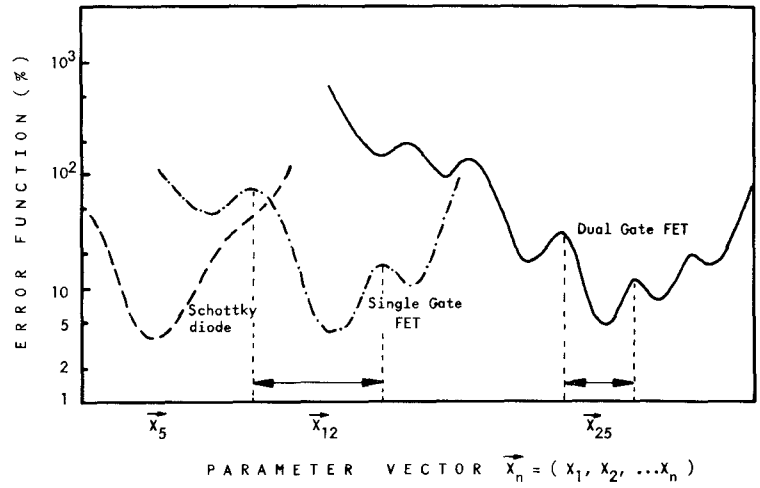

Fig. 7. Illustration of behavior of the error function EF (13) as a function of number of optimization parameters in the area of the global minimum. For starting vectors outside the indicated limits normally a local minimum instead of the desired global minimum will be found by the computer.

in parallel with the interelectrode capacitance C_{G1G2}. This type of circuit simulates exactly the gate 1 to gate 2 interaction in both directions and for both types of tested dual gate FET.

IV. Starting Values of the Optimization Procedure

A. General

Computer optimization is indispensable in order to find broad-band equivalent circuits of FET's. With an increasing number of optimization parameters, a set of good starting values is important since a) it simplifies the optimization procedure and saves computing time, and b) in some cases, it makes possible at all to find the global minimum, if the error function also has other local minima.

As illustrated in Fig. 7, it is obvious that in the case of 25 or more elements, the allowed uncertainty of the starting values is essentially smaller than it is the case with the 12 parameters of a single gate FET, whereas for the 5 elements of a Schottky diode, the computer, normally, should always find the global minimum.

A set of highly accurate starting values is therefore necessary for a straightforward determination of the equivalent circuit of a dual gate FET using optimization techniques. It is not evident that such a set of starting values will be possible to estimate using the formulas given in [5], [6], and [16], especially concerning the elements of the intrinsic FET's, since these can be calculated only if exact knowledge of mobility, doping density, and profile, as well as the effective thickness of the active layer, is provided. These data result from tedious material characterization measurements and are normally not available to the circuit designer. Knowledge of the exact bias conditions of the partial FET's is also indispensable and their calculation also needs these technological data.

Therefore, we divided the total optimization problem in four iterations: a) modeling of the gate 2 diode in forward bias (Fig. 8(a)); b) modeling of FET 1 (Fig. 8(b)); and c) modeling of FET 2 (Fig. 9). The results of the partial optimizations then serve as precise starting values for part (d), the overall dual gate FET optimization procedure (Fig. 6, Table I).

B. Partial FET's, Starting Values, and Equivalent Circuit

Estimation of starting values for the partial FET equivalent circuit has been carried out using relations already reported for single gate FET's modified for the case of the dual gate FET. The source and drain resistances follow from [17]

$$R_S = \left.\frac{\Delta V_{DS}}{\Delta I_{G1S}}\right|_{\text{floating: drain, gate 2}} \tag{5}$$

$$R_D = \left.\frac{\Delta V_{SD}}{\Delta I_{G2D}}\right|_{\text{floating: source, gate 1}} \tag{6}$$

The intergate resistance R_{12} follows from

$$R_{12} = \left.\frac{\Delta V_{DS}}{\Delta I_{G1D}}\right|_{\text{floating. source, gate 2}} - R_D = \left.\frac{\Delta V_{SD}}{\Delta I_{G2S}}\right|_{\text{floating: drain, gate 1}} - R_S. \tag{7}$$

The gate metallization resistances R_{G1} and R_{G2} can be estimated from the I–V characteristic of the corresponding real Schottky diode

$$V_{Gi} = I_{Gi} \cdot R_i + \frac{1}{\alpha_{0i}} \ln \frac{I_{Gi}}{I_{Si}}, \qquad i = 1,2 \tag{8}$$

where I_{Gi} is the diode current, R_i the static diode resistance, I_{Si} the saturation current, and $\alpha_{0i} \approx e/n_i kT$ a diode constant, to be determined from the ideality factor n_i of the gate diode. For $I_{Gi} > 1$ mA, the logarithmic plot of (8)

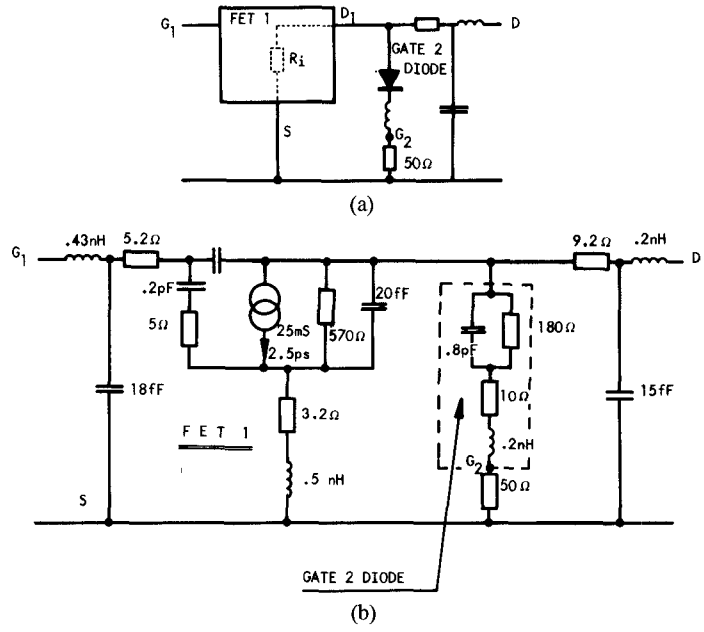

Fig. 8. Equivalent circuit of partial FET 1. For simulation of positively polarized gate 2 diode by means of S_{22}, FET 1 is replaced by a 500-Ω resistance (R_i).

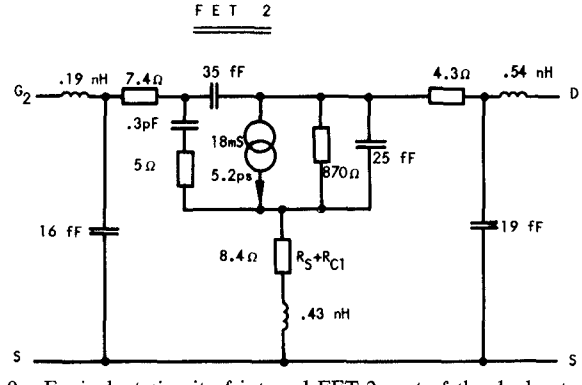

Fig. 9. Equivalent circuit of internal FET 2 part of the dual gate FET (a) valid for 2 to 11 GHz. R_{c1} is the open channel resistance of FET part 1.

is no more linear and the difference gives the value of $I_{Gi} \cdot R_i$ [18]. The HF values of R_{G1} and R_{G2} are lower than their dc values because of their distributed nature [14]. The gate series resistances can finally be estimated using the relation

$$R_{Gi} = \frac{R_i - R_x}{3}, \qquad \text{for} \begin{cases} i=1, & x=S \\ i=2, & x=D \end{cases}. \tag{9}$$

The input capacitances C_{GSi} of the two gates can be estimated from the imaginary part of the corresponding reflection coefficient S_{jj} measured for each partial FET separately, as will be described in Section IV-C, at 1 GHz according to [19]

$$C_{GSi} \approx -\frac{\mathrm{Im}\,(S_{jj})}{2\omega \cdot Z_0}, \qquad \begin{cases} i=1, & j=1 \\ i=2, & j=3 \end{cases} \tag{10}$$

where Z_0 is the characteristic impedance of the system (50 Ω). The transconductances g_{mi} can be estimated measuring under the same conditions the voltage gain S_{21} $(i=1)$ or S_{23} $(i=2)$ [19]

$$g_{m1} \approx \frac{|S_{21}|}{2Z_0 - R_S \cdot |S_{21}|} \qquad g_{m2} \approx \frac{|S_{23}|}{2Z_0 - R'_S \cdot |S_{23}|} \tag{11}$$

where R'_S is the open channel resistance of FET 1. Equations (10) and (11) are valid for lower frequencies when the input impedance of the device is capacitive and high in comparison to 50 Ω.

The channel resistances R_{Di} can be deduced from the slope of the saturation characteristics of each particular FET as given in Fig. 2. The interelectrode capacitances (intergate, source to gate 1, and drain to gate 2) were determined from contact dimensions and their distance using the nomograms given by Pucel *et al.* [16]. The starting values of the leading inductances (20–25-μm thick bonding wires) finally were estimated by measuring their length l_x according to the empirical formula

$$\frac{L_x}{\mathrm{nH}} \approx 0.7 \cdot \frac{l_x}{\mathrm{mm}}, \qquad x = G_1, G_2, D, S. \tag{12}$$

TABLE I

EQUIVALENT CIRCUIT ELEMENT VALUES OF DUAL GATE FET (a), (FIG. 4(a)), WITHOUT INTERGATE OHMIC CONTACT, AND DUAL GATE FET (b), (FIG. 4(b)), WITH INTERGATE OHMIC CONTACT, AS REFERRED TO THE CIRCUIT DESCRIBED IN FIGS. 5 AND 6. FOR DUAL GATE FET (a), BOTH PARTIAL FET'S ARE SATURATED WHEREAS FOR DUAL GATE FET (b), FET 1 IS NONSATURATED (V_{D1S} = 0.5 V)

	DEVICE / PARAMETER	DG. FET (a) : l_{G1} = 0.8 µm, l_{G2} = 2 µm Ext. bias : V_{DS} = 5V, V_{G1S} = -1V, V_{G2S} = +2V, I_D = 34 mA Int. bias : V_{D1S} = 2.1V, V_{DD1} = 2.9V, V_{G2D1} = -0.16V	DG. FET (b) : l_{G1} = 0.8 µm, l_{G2} = 0.8 µm V_{DS} = 5V, V_{G1S} = -1V, V_{G2S} = -1V, I_D = 12 mA V_{D1S} = 0.5V, V_{DD1} = 4.5 V, V_{G2D1} = - 1.5 V
FET n° 1	C_{GS1}	0.196 pF	0.165 pF
	R_{GS1}	9.7 Ω	15 Ω
	C_{GD1}	19.7 fF	24,6 fF
	g_{m1}	25.1 mS	20 mS
	τ_1	2.3 ps	2 ps
	R_{D1}	427 Ω	157 Ω
	C_{D1}	20.2 fF	23.2 fF
	R_{G1}	6.4 Ω	6.3 Ω
FET n° 2	C_{GS2}	0.284 pF	0.19 pF
	R_{GS2}	5 Ω	5.1 Ω
	C_{GD2}	33.2 fF	6 fF
	g_{m2}	16.5 mS	16.8 mS
	τ_2	4.8 ps	2 ps
	R_{D2}	854 Ω	876 Ω
	C_{D2}	11 fF	16.9 fF
	R_{G2}	5.4 Ω	5.4 Ω
Coupling of FET n° 1 and 2	R_{12}	4.9 Ω	7.5 Ω
	C_{G1G2}	5.6 fF	5.3 fF
Parasitics	R_S	3.4 Ω	5 Ω
	R_D	4.3 Ω	5.2 Ω
	L_{G1}	0.36 nH	0.26 nH
	L_{G2}	0.29 nH	0.3 nH
	L_S	0.42 nH	0.19 nH
	L_D	0.49 nH	0.28 nH
	C_{G1S}	6.6 fF	4.6 fF
	C_{G1D}	7.7 fF	2.3 fF
	C_{G2D}	3.8 fF	2.3 fF
	C_{DS}	3 fF	6.9 fF

The starting values of the parameters estimated using these relations permitted to enter the optimization procedure of the particular FET's with a value of the error function (EF, see (13)) of less than 20 percent. At the end of the optimization with EF≈5 percent, the values of the intrinsic FET's were introduced in the overall dual gate FET optimization, thus enabling a starting error EF of 15–19 percent.

Assuming that a solution of the optimization problem, i.e., an equivalent circuit of this form describing the HF behavior of the dual gate FET exists, then, according to Fig. 7, it should now be possible to find it by straightforward computer optimization.

C. Equivalent Circuit of Partial Single Gate FET's

In this section, the procedure will be described that permitted to gain "insight" into each one of the two single gate FET parts, that compose the dual gate FET.

Measurements of *S*-parameters of the partial FET's separately in their actual bias conditions have been possible using the transfer characteristic of Fig. 2. Starting with bias point P_1, we find the bias of each FET as follows:

a) FET 1: V_{D1S} = 2.1 V, V_{G1S} = −1 V, I_D = 34 mA
b) FET 2: V_{DD1} = 2.9 V, V_{G2D1} = −0.16 V, I_D = 34 mA.

Shifting now on the diagram to point P_2, FET 1 is nonsaturated and can be described by an ohmic resistance while FET 2 is biased as in (b), if we change externally the bias as follows: $V'_{DS} = V_{DD1} + V'_{D1S}$ = 2.9 V + 0.4 V = 3.3 V, V'_{G1S} = 0 V, $V'_{G2S} = V_{G2D1} + V'_{D1S}$ = −0.16 V + 0.4 V = 0.24 V, I_D = 34 mA.

S-parameters of FET 2 have been measured and its equivalent circuit has been determined using computer optimization (Fig. 9). Fig. 10 shows the comparison between measured and calculated *S*-parameters of FET 2.

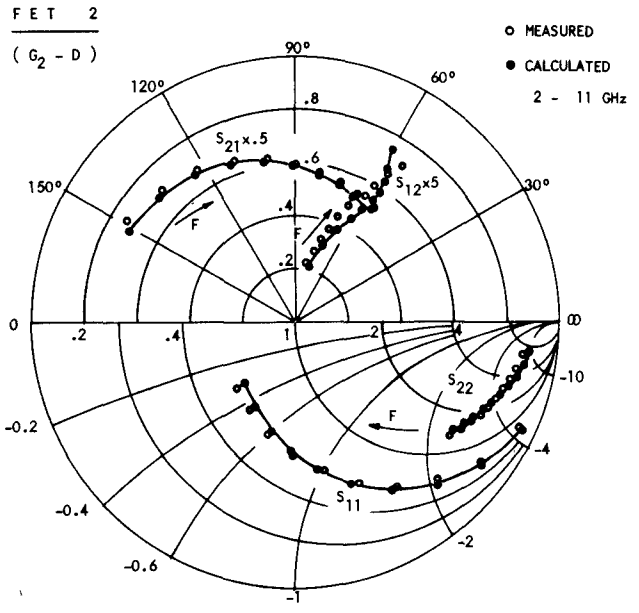

Fig. 10. Comparison of measured and calculated S-parameters of internal partial FET 2. Frequency: 2 –11 GHz. $\Delta f = 1$ GHz. Input port:gate 2, outport port:drain.

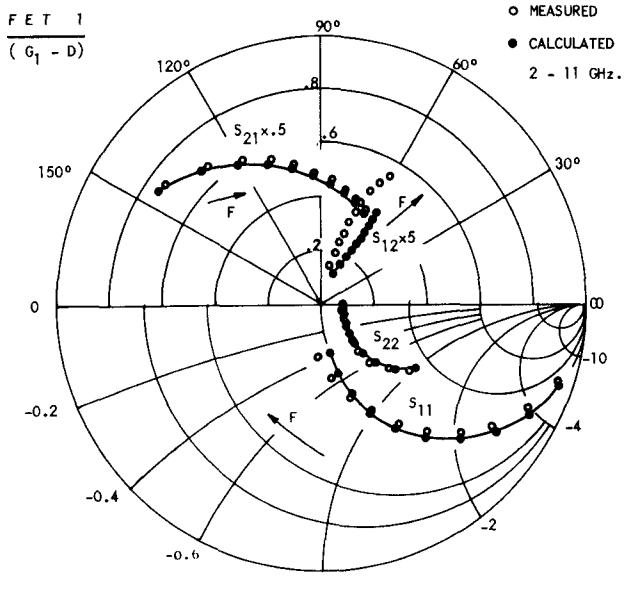

Fig. 11. Comparison of measured and calculated S-parameters of partial FET 1. Frequency: 2–11 GHz, $\Delta f = 1$ GHz. Input port:gate 1, output port:drain.

The gate 1 diode has no influence since it is mostly short-circuited by the open channel and the source resistance ($R_S + R_{c1}$) of FET 1.

The S-parameters of FET 1 can be measured if we shift with the bias to point P_3 (Fig. 2). For an overall bias of $V''_{DS} = V_{D1S} + V''_{DD1} = 2.1$ V $+0.4$ V $= 2.5$ V, $V''_{G1S} = -1$ V, $V''_{G2S} = V''_{G2D1} + V_{D1S} = 0.25$ V $+2.1$ V $= 2.35$ V, $I_D = 34$ mA, FET 2 is nonsaturated while FET 1 is in bias conditions as given in (a). In this case, however, the influence of the gate 2 diode has to be considered because of the 50-Ω load resistance at the drain.

Starting values of the Schottky-diode equivalent circuit have been estimated by simulating S_{22} and replacing FET 1 by its channel saturation resistance R_t of approximatively 500 Ω (Fig. 8(a)). Fig. 8(b) shows the equivalent circuit of FET 1. The resulting values of the parameters of the gate 2 diode are in good agreement with the theoretical predictions. The comparison between measured and calculated S-parameters of the first part of the dual gate FET is shown in Fig. 11.

The results of these two partial optimizations have subsequently served as starting values of the overall three-port optimization procedure.

The results of Section IV verify the assumption that a dual gate FET can be described efficiently by the cascode of two single gate FET's not only at dc but also at least for frequencies up to 12 GHz. This finding is in accordance with physical considerations and enables extension of the equivalent circuit of Section V to even higher frequencies.

V. Complete Equivalent Circuit of Dual Gate FET's

Three-port S-parameters of the dual gate FET have been measured with a computer controlled HP 8410 B network analyzer in the 2–11-GHz range. The FET's were mounted and bonded on a 10×10 mm^2 Al_2O_3 microstrip coplanar test fixture. Two ports have been used simultaneously, the third one being terminated by 50 Ω. The measurement of reflection coefficients is therefore carried out twice and has been a control means of the repeatability of the measurement. The "peeling" method has been used for de-embedding the FET and measuring exactly at the device plane [20]. S-parameters have been measured for different bias points and for the two types of FET's shown in Fig. 4. On each occasion, a preoptimization of the equivalent circuits of the partial FET's gave the final starting values. Using computer optimization (like simplex, multidimensional gradient, and random search) techniques, an error function defined by

$$\mathrm{EF} = \left\{ \sum_{f_k} \sum_{i,j} \frac{|S_{ij}\,\mathrm{meas} - S_{ij}\,\mathrm{calc}|^2}{\sum_{f_k} \sum_{i,j} |S_{ij}\,\mathrm{meas}|^2} \right\}^{1/2},$$

$$k = 1, \cdots, 10, \qquad (i,j) = (1,2,3) \tag{13}$$

has been minimized. Starting values of $\mathrm{EF}_{\mathrm{total}}$ were of the order of 15–19 percent because of using the results of preoptimization (see Fig. 7) and could be easily diminished to 4–5 percent. This was a good indication that the found minimum was the global one.

Optimization results of the two FET types are given in Table I, referring to the circuit of Figs. 5 and 6. Not all elements e_k of the equivalent circuit can be determined using this method with the same certainty. Since the measured data are S-parameters, those elements are most precisely calculated that have the major influence on the S-parameters. The error function EF (e_k) may have an

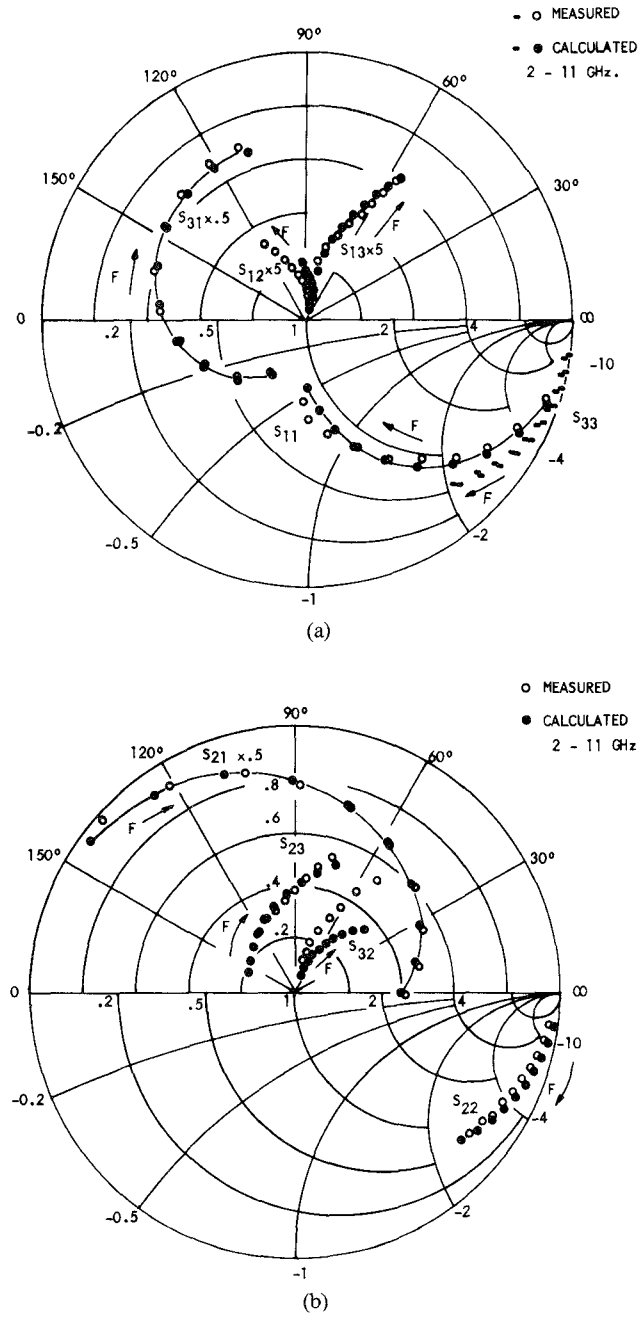

Fig. 12. Comparison of measured and calculated three-port S-parameters of complete dual gate FET of type (a). Bias as given by point P_1 in Fig. 2.

explicit minimum, as it is the case for $e_k = L_x$, g_{mi}, C_{GSi}, C_{GDi}, C_{G1G2}, and R_S. For some other elements ($e_k = R_{GSi}$, R_D, R_{Gi}, C_{G1S}, C_{G2D}, and R_{Di}) the function EF (e_k) has a rather flat minimum and these elements can be determined with only limited precision.

The comparison of measured and calculated S-parameters given in Fig. 12(a) and (b) show a good agreement for most of the nine S-parameter sets. Extrapolation to 12 or 13 GHz is justifiable as the good coincidence up to 11 GHz shows. Similar results were obtained for FET of type (b). Only the feedback parameters S_{12} and S_{32} between the two gates and the drain have been difficult to simulate over the whole frequency range, but this stems from the small magnitude and the resulting influence of crosstalk in the microwave test fixture at frequencies higher than 6 GHz.

Coupling between the two FET parts could be described for both types of dual gate FET by the same R_{12} C_{G1G2} circuit (parameter S_{13} and S_{31}). The intergate ohmic contact of dual gate FET (b) forms a short-circuit with the active layer beneath it for dc as well as for high frequencies up to 11 GHz, as the corresponding values of R_{12} in Table I in relation with the FET geometry of Fig. 4 indicate.

All other parameter values given in Table I correspond well to the geometrical and technological differences between the two dual gate FET's (a) and (b). In dual gate FET (a) they represent the differences in geometry of the two gates and in dual gate FET (b) the different bias conditions of the otherwise identical partial FET's 1 and 2.

If FET's with more than two gates are considered, the proposed method can also be applied in order to determine the wide-band equivalent circuit as far as the corresponding multidimensional transfer characteristic of the device can be deduced.

VI. Summary

Modeling of GaAs dual gate MESFET's at microwave frequencies between 2 and 11 GHz is reported. The found model for two FET's of different technology and geometry consists of 28 frequency independent elements, describes fairly well measured three-port S-parameters to 11 GHz, the physical and geometrical properties of the devices, and is extendable to 13 GHz. The indispensable accurate starting values for the optimization could be estimated using a new modeling method: it consists of separate dc and HF characterization (S-parameters) as well as equivalent circuit determination of each FET part of the dual gate FET and of the gate 2 diode.

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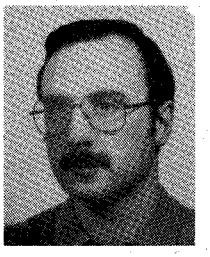

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Numerical Analysis of Nonlinear Solid-State Device Excitation in Microwave Circuits

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Abstract — **This paper presents an efficient technique for the numerical determination of voltage and current waveforms when a microwave circuit containing one or more nonlinear elements is excited by a single frequency source. The approach described here is readily applied to microwave networks represented by a large number of equivalent circuit elements, either lumped or distributed. A significant feature of this paper is the detailed investigation of the problem of convergence, using this new technique. The generality of the technique is illustrated through its application to studies of the excitation of varactor, Schottky-barrier, and IMPATT diodes in waveguide circuits. In addition, the relationship of this method to the multiple reflection approach is discussed and the convergence mechanism of this reflection technique is studied.**

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I. INTRODUCTION

THIS PAPER reports a general method for the analysis of microwave circuits which contain a sinusoidal source and one or more nonlinear devices. It is applicable to the

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